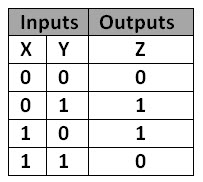
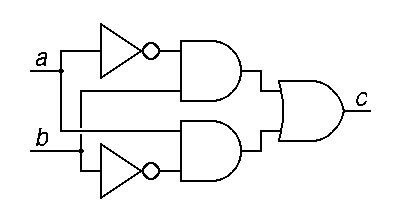
**Circuit Diagram & Truth Table:**

****

**z=x’y+xy’**

**Code:**

* **Design Module**

module gate(z,x,y);

input x,y;

output z;

wire a,b,xb,yb;

not n1(xb,x);

not n2(yb,y);

and a1(a,xb,y);

and a2(b,yb,x);

or o1(z,a,b);

endmodule

* **TestBench**

module baig;

reg x,y;

wire z;

gate g1(z,x,y);

initial

begin

x=1'b0;y=1'b0;

#20

x=1'b0;y=1'b1;

#20

x=1'b1;y=1'b0;

#20

x=1'b1;y=1'b1;

#20

$finish;

end

endmodule

**Output:**

